Assignment 2 Coursework Specification

Module name:	**Advanced Digital Design**
Module code:	**ENGD3001**
Title of the Assignment:	**Assignment 2**
This coursework item is:	**Formative**
This coursework will be marked anonymously:	**Yes**

The module learning outcomes that are assessed by this coursework are:

1. "Knowledge and specialist analytic development techniques in the areas of VLSI design, ASM design and implementation, and VHDL design."
2. "Development of generic and transferable skills in advanced digital system design methodologies using industry standard design tools."

This coursework is:	**Individual**

This coursework constitutes 60% to the overall module mark.

When completed you are required to submit the following:

Submit an electronic copy of your assignment via Blackboard by the advertised deadline.

Please note that once a submission is made it is final. No resubmissions or later additions are allowed under any circumstances, so please ensure that your report is correct and complete before submitting it.

Your marked coursework and feedback will be available to you on: If for any reason this is not forthcoming by the due date your module leader will let you know why and when it can be expected.	**10 June 2022**

Late submission of coursework policy:

Late submissions will be processed in accordance with current University regulations which state:

*"The time period during which a student may submit a piece of work late without authorisation and have the work capped at 40% [50% at PG level] if passed is **14 calendar days**. Work submitted unauthorised more than 14 calendar days after the original submission date will receive a mark of 0%. These regulations apply to a student's first attempt at coursework. Work submitted late without authorisation which constitutes reassessment of a previously failed piece of coursework will always receive a mark of 0%."*

Academic Offences and Bad Academic Practices:

These include plagiarism, cheating, collusion, copying work and reuse of your own work, poor referencing or the passing off of somebody else's ideas as your own. If you are in any doubt about what constitutes an academic offence or bad academic practice you must check with your tutor. Further information and details of how DSU can support you, if needed, is available at:

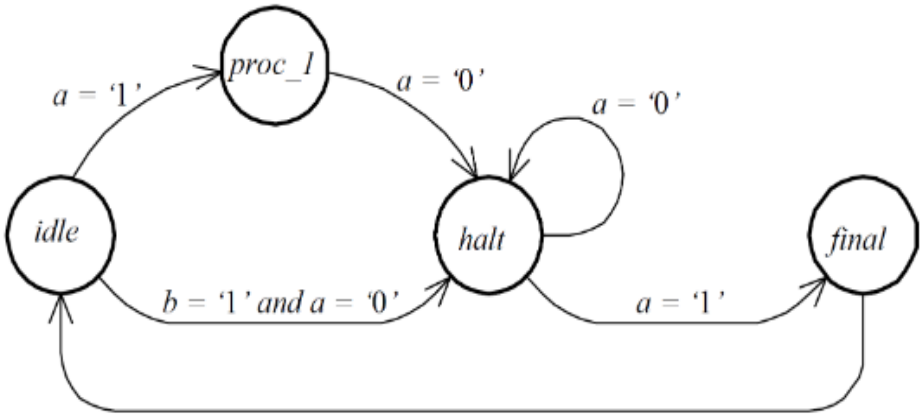
https://www.dmu.ac.uk/current-students/student-support/exams-deferrals-regulations-policies/student-regulations-and-policies/academic-offences.aspx

and

https://www.dmu.ac.uk/current-students/student-support/exams-deferrals-regulations-policies/student-regulations-and-policies/bad-academic-practice.aspx

Assignment 2

The figure below shows the state transition diagram of a finite state machine (FSM) and its intended operation.



The outputs of the FSM are defined in the following table:

STATES / OUTPUTS	*idle*	*proc_1*	*halt*	*final*
main	000	100	010	001
fsm	0	0	0	1

Simulate this design **with the aid of a "graphical testbench"** (also known as a "Test Bench Waveform" file), **using the Xilinx ISE v10.1.03 software**. You must set the colour scheme of your simulation waveforms to the "**Classic**" colour scheme, via the 'Edit' → 'Preferences...' → 'ISE Simulator (ISim)' → 'Simulation Waveform Colors' menu.

It is a mandatory requirement of this assignment to use the correct software version and the correct type of testbench, using the required colour scheme.

What you should submit

You should submit a formal technical report explaining your design and your results.

Specifically, your report should contain at least the following information:

a) An introduction, including the design brief,
b) A background section on FSMs, their various types and their operation,
c) A design section explaining how you've solved the design task handed out to you and if applicable why you've selected a particular solution out of several possible,
d) The complete listing of the VHDL code, **bearing in mind good programming practice and FSM design recommendations**,
e) A legible screenshot of your graphical testbench,
f) The results of the simulations (i.e. suitable, legible and detailed simulation waveforms) accompanied by detailed comments and explanations, and
g) Conclusions (and possible further improvements if applicable).

Please ensure that you design your testbench in such a way that it comprehensively verifies all possible states/transitions of the FSM.

For general guidance on writing (technical) reports please refer to the following links:

https://www.theiet.org/media/5182/technical-report-writing.pdf
https://library.dmu.ac.uk/ld.php?content_id=31952526
https://library.dmu.ac.uk/class/HEAT

There are no set word limits for this assignment, therefore please use appropriate judgement to convey the necessary information by striking the appropriate balance for each section in order to fulfil the requirements of the assignment.

For full marking details please consult the associated marking scheme from Blackboard.

 Please also make sure that you carefully read the corresponding **Blackboard announcement** and pages 6-7 of the **ENGD3001 Module Handbook** which contain important information, advice and guidelines regarding your assignments.